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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	14

DATE MAILED: 11/04/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

PRG

Office Action Summary	Application No.	Applicant(s)	
	09/505,949	CHOW ET AL.	
	Examiner	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 August 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-19 have been considered. Claim 18 has been amended as per Applicant's request.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) do not apply to the examination of this application as the application being examined was not (1) filed on or after November 29, 2000, or (2) voluntarily published under 35 U.S.C. 122(b). Therefore, this application is examined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1-4, 6, 8, 10-16, and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Blomgren et al., U.S. Patent Number 5,884,057 (herein referred to as Blomgren).

5. In regards to claim 1, Blomgren has taught a processor comprising:

   a. A first instruction set engine to process instructions from a first instruction set architecture (ISA) having a first word size (Blomgren column 6, lines 37-38 and Figure 4, element 36).

   b. A second instruction set engine to process instructions from a second ISA having a second word size (Blomgren column 6, lines 37-38 and Figure 4,

element 32), the second word size being difference than the first word size (Blomgren column 6, lines 40-42).

c. A mode identifier (Blomgren column 6, lines 45-46 and Figure 4, element 38).

d. A plurality of floating-point registers shared by the first instruction set engine and the second instruction set engine (Blomgren column 7, lines 50-52 and Figure 4, element 20).

e. A floating-point unit coupled to the floating-point registers, the floating-point unit processing an input responsive to the mode identifier to produce an output (Blomgren column 2, lines 60-63 and Figure 4, element 14).

6. In regards to claim 2, Blomgren has taught a processor wherein the mode identifier is one of a plurality of bits in a processor status register (Blomgren column 6, lines 45-46 and Figure 4, element 38). Regarding Blomgren, the mode identifier was stored in the mode register, which functions similarly to the status register.

7. In regards to claim 3, Blomgren has taught floating-point unit comprising:

a. Pre-processing hardware to detect if a token exists in the input (Blomgren column 6, lines 64-65 and column 7, lines 11-14).

b. An arithmetic unit responsive to the input and the mode identifier (Blomgren column 5, lines 42-48). Regarding Blomgren, an arithmetic unit would complete the operations cited.

c. Post-processing hardware to perform a token specific operation if a token exists in the input (Blomgren column 7, lines 5-10 and 11-14).

8. In regards to claim 4, Blomgren has taught a processor wherein the input includes data stored in at least one of the floating-point registers (Blomgren column 7, lines 56-59).

9. In regards to claim 6, Blomgren has taught a processor wherein the token represents a "not a thing value" (NaTVal) that defines an unsuccessful speculative load request (Blomgren column 2, lines 23-25; column 3, lines 12-14; and columns 6-7, lines 61-14). Regarding Blomgren, the token signifies when improper data was loaded from the registers, and Blomgren recognizes this occurrence with CISC instructions. He identifies the CISC instructions that would load improper data if they tried to load data from the registers in a way similar to the tokens described by the applicant.

10. In regards to claim 8, Blomgren has taught a processor wherein the mode identified indicates whether the processor is in a first mode or a second mode (Blomgren column 2, lines 60-63 and column 6, lines 45-46).

11. In regards to claim 10, Blomgren has taught a method in a processor comprising:

a. Fetching an input from at least one of a plurality of floating-point registers (Blomgren column 7, lines 56-59).

b. Detecting whether the input includes a token (Blomgren column 6, lines 64-65).

c. If the token is detected in the input, check what mode the processor is in (Blomgren columns 6-7, lines 45-14 and columns 10-11, lines 58-59).

d. If the processor is in a first mode, process the input to render an arithmetic result (Blomgren column 5, lines 40-49 and columns 6-7, lines 61-10).

e. If the processor is in a second mode, perform a token specific operation (Blomgren column 7, lines 5-10 and 11-14).

f. Producing an output (Blomgren column 5, lines 48-49).

12. In regards to claim 11, Blomgren has taught a method:

a. Wherein the input is comprised of at least one operand (Blomgren column 2, lines 41-43) and at least one operator (Blomgren column 5, lines 44-45). Regarding Blomgren, it was inherent that the input contains an operator, because it would specify which floating-point operation to complete.

b. Wherein detecting comprises examining the at least one operand to determine whether any of the operands corresponds to the token (Blomgren column 6, lines 64-65).

c. Wherein checking comprises examining a mode identifier to determine whether the processor is in the first mode or the second mode (Blomgren column 2, lines 60-63 and column 6, lines 56-59).

13. In regards to claim 12, Blomgren has taught a method wherein processing comprises executing at least one operation on the at least one operand according to the at least one operator to achieve a result (Blomgren column 5, lines 40-49).

14. In regards to claim 13, Blomgren has taught a method wherein performing comprises propagating the token; and wherein producing output comprises setting the output to be the token (Blomgren columns 6-7, lines 61-14). Regarding Blomgren, the token signifying that the instruction was a CISC instruction must be propagated through in order for the processor to recognize that it was a CISC instruction not a series of RISC

instruction. The output would be set to the token when the token represented a stall, so that no data would be outputted.

15. In regards to claim 14, Blomgren has taught a method wherein the token represents a "not a thing value" (NaTVal) that defines an unsuccessful speculative load request (Blomgren column 2, lines 23-25; column 3, lines 12-14; and columns 6-7, lines 61-14).

16. In regards to claim 15, Blomgren has taught a method wherein checking comprises checking a mode identifier (Blomgren column 2, lines 60-63 and column 6, lines 56-59).

17. In regards to claim 16, Blomgren has taught a method wherein checking comprises checking a mode identifier bit in a processor status register (Blomgren column 6, lines 45-46 and Figure 4, element 38).

18. In regards to claim 19, Blomgren has taught a method in a multi-mode processor (Blomgren column 10, lines 16-22) comprising:

a. Fetching an input from at least one of a plurality of floating-point registers (Blomgren column 7, lines 56-59).

b. Detecting whether the input includes at least one token of a plurality of tokens (Blomgren column 6, lines 64-65).

c. If at least one token is detected in the input, check what mode the processor is in (Blomgren column 6, lines 45-51; columns 6-7, lines 61-10; and column 7, lines 11-14).

d. Processing the input to render an arithmetic result when the processor is in at least a first mode of a plurality of modes (Blomgren column 5, lines 40-49 and columns 6-7, lines 61-10).

e. Performing a token specific operation when the processor is in at least a second mode of a plurality of modes (Blomgren column 7, lines 5-10 and 11-14).

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blomgren et al., U.S. Patent Number 5,884,057 (herein referred to as Blomgren) in view of Dao et al., U.S. Patent Number 6,148,395 (herein referred to as Dao). Blomgren has taught a processor in claim 1 (see above) wherein the input may contain a token (Blomgren column 6, lines 61-67) and wherein the token being an 82 bit processor known value. Blomgren does not explicitly teach the token is an 82 bit processor value, however the size of the token does not matter because it functions the same. See *In re Rose*, 105 USPQ 237, 240 (CCPA 1955) (herein referred to as *In re Rose*).

21. Blomgren has not taught wherein the floating-point registers are 82 bits wide. Dao has taught floating-point registers capable of storing floating-point data in the maximum available precision (Dao column 8, lines 10-12). It would have been obvious to a person of ordinary skill in the art to make the floating-point registers as wide as

feasibly possible, because it would increase the precision of the data. Therefore it would have been obvious to a person of ordinary skill in the art at the time this invention was made to make the floating-point registers in the invention of Blomgren as wide as feasibly possible, as taught by Dao, in order to increase precision of the floating-point operations. Also, the exact number of bits does not matter. See *In re Rose*.

22. Claims 7, 9, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Blomgren et al., U.S. Patent Number 5,884,057 (herein referred to as Blomgren) in view of IEEE Standard for Binary Floating-Point Arithmetic (herein referred to as IEEE).

23. In regards to claim 7, Blomgren has taught floating point registers each comprising an exponent and a significand (Blomgren column 10, lines 31-33). Blomgren has not taught a sign bit. IEEE has taught a sign bit is part of the basic floating-point format (IEEE page 4, section 3.2). It would have been obvious to a person of ordinary skill in the art to incorporate the sign bit in the sign bit, because it would assure compatibility with outside programs and devices written and built according to the IEEE standard. Therefore it would have been obvious to a person of ordinary skill in the art at the time this invention was made to incorporate the sign bit, as taught by IEEE, in the registers of Blomgren to increase compatibility.

24. In regards to claims 9 and 17, Blomgren has not explicitly taught a processor wherein the mode identifier indicates whether the processor is in a 32 bit word ISA mode or a 64 bit word ISA mode (Applicant' Claim 9) nor a method wherein the first mode is a 32 bit word ISA mode and the second mode is a 64 bit ISA mode (Applicant's Claim 17). However Blomgren has taught that any type of instruction set may be used (Blomgren column 10, lines 16-22). IEEE has taught that the floating-point standard formats are 32

bits or 64 bits wide. It would have been obvious to a person of ordinary skill in the art to use instruction sets of 32 bits and 64 bits, because these two instruction sets would be compatible with any outside program or device written or built to be compatible with the IEEE standards. Therefore, it would have been obvious to a person of ordinary skill in the art at the time this invention was made to use the instructions with the IEEE standards of 32 bit and 64 bit words in the invention of Blomgren to increase compatibility. Also, the actual word size of the instruction set does not matter. See *In re Rose*.

25. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Blomgren et al., U.S. Patent Number 5,884,057 (herein referred to as Blomgren) in view of Kohn, U.S. Patent Number 5,204,828 (herein referred to as Kohn). Blomgren has taught a multi-mode processor (Blomgren column 10, lines 16-22) comprising:

a. A plurality of instruction set engines to process instructions from a plurality of instruction set architectures having different word sizes (Blomgren column 6, lines 37-38; column 10, lines 16-22; and Figure 4, elements 32 and 36).

b. A mode identifier (Blomgren column 6, lines 45-46 and Figure 4, element 38).

c. A plurality of floating-point registers shared by the first instruction set engine and the second instruction set engine (Blomgren column 7, lines 50-52 and Figure 4, element 20).

d. A floating-point unit coupled to the floating-point registers, the floating-point unit processing an input responsive to the mode identifier to produce an output (Blomgren column 2, lines 60-63 and Figure 4, element 14).

26. Blomgren has not taught a plurality of floating-point units. Kohn has taught a plurality of floating-point units. It would have been obvious to a person of ordinary skill in the art to include multiple floating-point units, because multiple floating-point units would achieve faster execution speeds. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate multiple floating-point units, as taught by Kohn, in the invention of Blomgren to increase execution rates.

Response to Arguments

27. Applicant's arguments filed 15 August 2003, Paper Number 13, have been fully considered but they are not persuasive.

28. Applicants argue on pages 5-6 and 10-11 essentially

> "Applicants submit that the teachings of Blomgren are limited to processing opcodes of different lengths. Applicants submit that there is no suggestion as to any variation in the word sizes between the RISC and CISC instruction sets within Blomgren."

29. This has not been found persuasive. The RISC and CISC instruction sets are inherently different sizes, as asserted in prior office actions. Extrinsic evidence from Hennessy and Patterson's Computer Architecture: A Qualitative Approach ©1997 was provided with the last office action towards this effect. Hennessy states on page 91, section 3.2.1, paragraph 2 "**General Characteristics of CISC machines**...The result is instructions that are of ***widely varying lengths*** and execution times." He also states on page 93, section 3.2.3, paragraph 3 "**Fixed Instruction Length** If one instruction is to issue per clock cycle, it is natural that ***RISC designers would limit all instructions to a***

fixed length, usually 1 word." Relevant portions of are cited and specific characteristics are highlighted. As can be seen by the quotes from Hennessy and Patterson, CISC and RISC instructions sets are different sizes, since CISC has instructions of varying lengths and RISC has fixed length instructions.

30. Applicants argue on page 6 essentially "Applicants submit that the cited passages implies that the instruction word size is the same for both the CISC and RISC instruction sets." This has not been found persuasive. The passage cited by the Applicants can, at most, not relate to instruction word size. The interpretation submitted above ignores the inherent principles and facts about RISC and CISC instruction sets, as set forth above and in Hennessy and Patterson. The passage taken in light of the inherent attributes, as stated in Hennessy and Patterson, of RISC and CISC instruction sets is an example of why the RISC and CISC instruction sets are different sizes.

31. Applicants argue on pages 6-7 essentially

> "...Applicants respectfully submit that Blomgren teaches the selection of decoded instructions from one of a CISC instruction set architecture or an RISC instruction set architecture, depending on a mode indicated by a mode register. Conversely, Claim 1 requires processing of a data input responsive to the mode identifier."

32. This has not been found persuasive. The claim language states "a floating-point unit coupled to the floating-point registers, the floating-point unit processing an input responsive to the mode identifier to produce an output." This has been interpreted to mean that the floating-point unit processes input according to what has been specified by the mode identifier. The mode identifier in Blomgren specifies which instruction is to be

executed by the floating-point unit, which executes a process on an input in accordance with the instruction to produce an output. The instruction also defines which operands will be operated on by the floating-point unit, so if the mode identifier controls which process and data will be operated on. Blomgren's floating-point unit processes data input responsive to the mode identifier, since the mode identifier selects an instruction, which defines which process is to be executed on what data.

33. Applicants argue on pages 7-9 essentially

> "As is clearly indicated by the cited passage, there is no reference to whether a check of whether a token is received as a data input...
>
> ...
>
> ...Applicants respectfully submit that the instruction emulation as taught by Blomgren does not provide any teachings or suggestions with reference to processing of tokens received as data input operands when in a first mode and processing a token specific operation when the processor is in a second mode..."

34. This has not been found persuasive. The exact claim language is "detecting whether the input includes a token". Applicants' arguments are based around the assumption that "includes" has the same definition and scope as "contains". "Includes" does not necessarily mean that the token is found within the input read from the floating-point register, just that there is a token associated with the input. Also, "includes" has a broader scope than "contains", and, if the claim had stated "detecting whether the input contains a token," then Applicants' arguments would be persuasive and correct. Blomgren has taught that there is a token, which defines the instruction and data as RISC

or CISC and floating-point or integer throughout the entire system. This is how the system differentiates between RISC and CISC and floating-point and integer. When Blomgren is in CISC mode, input data is read directly from memory into the floating-point registers and operated upon. When Blomgren is in RISC mode, the input data must first be read into the integer general purpose registers (INT GPR), then the data is transferred to the floating-point registers before it can be inputted into the floating-point unit (Blomgren column 7, lines 50-64). Throughout this entire process, the data is marked as floating-point or integer data as well as whether the mode is RISC or CISC so the input data can be processed correctly.

Conclusion

35. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Hammond et al., U.S. Patent Number 5,638,525, has taught a device that processes two instructions sets of differing sizes.

b. Trivedi et al., U.S. Patent Number 6,430,674 has taught a device that processes multiple instruction set architectures.

36. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (703) 305-7596. The examiner can normally be reached on M-T 7:30am-5:00pm.

37. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 746-7239 for regular communications and (703) 746-7238 for After Final communications.

38. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Aimee J. Li
Examiner
Art Unit 2183

October 29, 2003

EDDIE CHAN
SUPERVISORY PATENT EXAMINER
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